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TO: **Examiner Amine Riad**	FROM: **Justin Liu** Reg. No. 51,959
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Please see attached Unofficial Communication.

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PATENT
UNOFFICIAL COMMUNICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Brendan K. Bridgford		
Assignee:	Xilinx, Inc.		
Title:	"A Method of Debugging PLD Configuration Using Boundary Scan"		
Serial No.:	10/606,728	Filing Date:	06/26/2003
Examiner:	Amine Riad	Art Unit:	2113
Docket No.:	X-1216 US	Conf. No.:	5830

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UNOFFICIAL COMMUNICATION

Pursuant to a telephone conversation with the Examiner on May 14, 2008, Applicant submits the following proposed amended claims. For clarity and simplicity, amendments to only the independent claims are presented. This communication is unofficial and provided only for the purposes of discussion. Please contact me if I can provide any further assistance at 408-879-4641.

Respectfully submitted,

/Justin Liu 51,959/

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Proposed Claim Amendments

1. (Currently Amended) A method for debugging a configuration process of a device having programmable logic and a JTAG interface comprising:

providing a first connection between a configuration device and the device having programmable logic through the JTAG interface;

providing a second connection between [[a]] the configuration device and an input/output pin of the device having programmable logic which is separate from the JTAG interface;

initiating the configuration process for the device having programmable logic;

coupling configuration process signals to the input/output pin of the device having programmable logic;

using boundary scan registers of the device having programmable logic to capture the configuration process signals received at the input/output pin of the device during the configuration process;

using the boundary scan registers to transfer the captured configuration process signals to a configuration analyzer during the configuration process;

analyzing the transferred configuration process signals using the configuration analyzer; and

verifying the second connection between the configuration device and the input/output pin of the device having programmable logic coupled to receive the configuration process signals.

9. (Currently Amended) A system comprising:

a device having programmable logic and a JTAG interface coupled to boundary scan registers, the device coupled to receive a configuration bitstream by way of an input/output (I/O) pin separate from the JTAG interface;

a configuration device coupled to the I/O pin of the device having programmable logic for providing the configuration bitstream to the device having

programmable logic by way of the I/O pin, the configuration device further separately coupled to the device having programmable logic via through the JTAG interface; and

a configuration analyzer coupled to the configuration device for driving configuration process signals through the configuration device in single steps, and coupled to the device having programmable logic for controlling I/O pins of the device having programmable logic and analyzing configuration process signals stored in the boundary scan registers of the device having programmable logic during the configuration process;

wherein the device having programmable logic, the configuration device, and the analyzer form at least part of a JTAG chain enabling verifying a connection to the input/output pin of the device having programmable logic coupled to receive the configuration bitstream.

16. (Currently Amended) A machine readable storage having stored thereon, a computer program having a plurality of code sections for debugging a configuration process of a device having programmable logic and a JTAG interface, the code sections executable by a machine for causing the machine to perform the steps of:

initiating the configuration process for the device having programmable logic;

coupling JTAG signals to the JTAG interface of the device having programmable logic;

coupling configuration process signals to an input/output pin of the device having programmable logic, wherein the input/output pin is separate from the JTAG interface;

using boundary scan registers of the device having programmable logic to capture the configuration process signals received at the input/output pin of the device having programmable logic during the configuration process;

using the boundary scan registers to transfer the captured configuration process signals to a configuration analyzer during the configuration process;

analyzing the transferred configuration process signals using the configuration analyzer; and

verifying a connection to the input/output pin of the device having programmable logic coupled to receive the configuration process signals.

17. (Currently Amended) A configuration analyzer for debugging a configuration process of a device having programmable logic and a JTAG interface comprising:

means for receiving JTAG signals by way of the JTAG interface of the device having programmable logic;

means for receiving configuration process signals by way of an input/output pin of the device having programmable logic separate from the JTAG interface;

means for stepping through the configuration process;

means for capturing configuration process signals received at the input/output pin in boundary scan registers as the configuration process signals are received by the device having programmable logic at each step;

means for comparing the captured configuration process signals output by the boundary scan registers in a JTAG chain with expected configuration process signals during the configuration process; and

means for verifying a connection to the input/output pin of the device having programmable logic coupled to receive the configuration process signals.